Lab 3 Report

Time Spent on Lab: 7hours

State transition diagram图示

描述已自动生成:

图形用户界面, 文本, 应用程序

描述已自动生成Structural SystemVerilog code:

电脑萤幕画面

描述已自动生成Simulation waveforms:

This is a testbench for 2 complete cycles for both left and right. The reset input starts at the first positive edge. The first Left input is entered at the second negative edge. After half a clock cycle, la turns on followed by lb and lc. After lc turns on a cycle, left is reset. After a cycle, right turns on. Then, ra turns on. Rb and rc follows as well. Then, I set once a again a complete cycle for both left and right. The results are as my expectrations.

电脑屏幕的地图

描述已自动生成RTL Viewer schematics:

Behavioral SystemVerilog code:

电脑萤幕的截图

描述已自动生成

图形用户界面, 文本, 应用程序

描述已自动生成图形用户界面, 文本, 应用程序

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